UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/305,240	05/04/99	SHIM B	5484-48

MMC1/0417
MARGER JOHNSON & MCCOLLOM P C
1030 S W MORRISON STREET
PORTLAND OR 97205

EXAMINER	
NADAV,O	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 04/17/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trad marks

Office Action Summary	Application No. 09/305,240	Applicant(s) Shim et al.
	Examiner ORI NADAV	Group Art Unit 2811

☒ Responsive to communication(s) filed on *Mar 17, 2000* .

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-9* is/are pending in the application.

Of the above, claim(s) *1-4* is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *5-9* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☒ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Election/Restriction

1. Applicant's election without traverse of claims 5-9 in Paper No. 4 is acknowledged.

Specification

2. The disclosure is objected to because of the following informalities: On page 2, line 8, "in series each other" should read "in series to each other".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kosa et al. (4,764,479) in view of Admitted Prior Art (APA).

Kosa et al. teach in figure 18 a pull up transistor comprising: a semiconductor substrate 10, of a first conductivity type, source and drain regions of a second conductivity type formed in the substrate and defining a channel region therebetween, a wiring connected to the source and drain regions, an impurity implantation region of impurities of a second conductivity type N- in a first sector of the channel region, the first sector reaching at most one of the source and drain regions, a gate insulating layer 16d on the substrate and over at least a portion of the impurity implantation region and over at least a portion of an area adjacent the impurity implantation region, and a gate G3 on the gate insulating layer over at least a portion of the first sector and of a region adjacent to the first sector, wherein the first sector has a narrower line width than a line width of the gate and the first portion is in a predetermined ratio with the area adjacent to the first portion.

Kosa et al. do not disclose one of the source and drain regions being coupled with the I/O pad and the other one being coupled with the Vdd terminal.

APA teaches in figure 1 a pull up transistor, wherein one of the source and drain regions being coupled with the I/O pad and the other one being coupled with the Vdd terminal.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to connect one of the source and drain regions being coupled with the I/O pad and the other one being coupled with the Vdd terminal in Kosa et al.'s device in order to operate the transistor in its intended use as an enhancement mode transistor.

5. Claims 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nandakumar et al. (5,917,219) in view of Admitted Prior Art (APA).

Nandakumar et al. teach in figure 3A a transistor for use as a pull up transistor with a Vdd terminal and an I/O pad of a semiconductor device comprising: a semiconductor substrate 62, of a first conductivity type, source and drain regions 56, 58 of a second conductivity type formed in the substrate and defining a channel region therebetween, an impurity implantation region 66 of impurities of a second conductivity type N+ in a first sector of the channel region, the first sector does not reach either one of the source and drain regions and is separated therefrom by equal distances, a gate insulating layer 54 on the substrate and over at least a portion of the impurity implantation region and over at least a portion of an area adjacent the impurity implantation region, and a gate 52 on the gate insulating layer over at least a portion of the first sector and of a region adjacent to the first sector, wherein the first sector has a narrower line width than a line width of the gate and the first portion is in a predetermined ratio with the area adjacent to the first portion.

Nandakumar et al. do not teach using the transistor as a pull up transistor in which one of the source and drain regions being coupled with the I/O pad and the other one being coupled with the Vdd terminal.

APA teaches in figure 1 a pull up transistor, wherein one of the source and drain regions being coupled with the I/O pad and the other one being coupled with the Vdd terminal.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Nandakumar's transistor as a pull up transistor, in which one of the source and drain regions being coupled with the I/O pad and the other one being coupled with the Vdd terminal, because it is conventional to connect one of the source and drain regions being coupled with the I/O pad and the other one being coupled with the Vdd terminal in a pull up transistor in order to operate the transistor in its intended use as an enhancement mode transistor.
Furthermore, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References C-E are cited as being related to impurity implantation regions.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group

2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 3 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

Tom Thomas

Tom Thomas
Supervisory Patent Examiner
Technology Center 2800

Ori Nadav, Ph.D.

April 14, 2000